JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA
KAKINADA – 533 003, Andhra Pradesh, India
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II Year - I Semester		L	T	P	C
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SWITCHING THEORY AND LOGIC DESIGN LAB					

List of Experiments: (Minimum of Twelve Experiments has to be performed)

1. Verification of truth tables of Logic gates
   Two input (i) OR (ii) AND (iii) NOR (iv) NAND (v) Exclusive OR
   (vi) Exclusive NOR
2. Design a simple combinational circuit with four variables and obtain minimal SOP expression and verify the truth table using Digital Trainer Kit
3. Verification of functional table of 3 to 8 line Decoder/De-multiplexer
4. 4 variable logic function verification using 8 to1 multiplexer.
5. Design full adder circuit and verify its functional table.
6. Verification of functional tables of
   (i) JK Edge triggered Flip–Flop (ii) JK Master Slav Flip–Flop (iii) DFlip-Flop
7. Design a four bit ring counter using D Flip–Flops/JK Flip Flop and verify output
8. Design a four bit Johnson's counter using D Flip-Flops/JK Flip Flops and verify output
9. Verify the operation of 4-bit Universal Shift Register for different Modes of operation.
10. Draw the circuit diagram of MOD-8 ripple counter and construct a circuit using T- Flip-Flops and Test it with a low frequency clock and Sketch the output wave forms.
11. Design MOD–8 synchronous counter using T Flip- Flop and verify the result and Sketch the output wave forms.
12. (a) Draw the circuit diagram of a single bit comparator and test the output
    (b) Construct 7 Segment Display Circuit Using Decoder and 7 Segment LED and test it.

ADDon Experiments:

1. Design BCD Adder Circuit and Test the Same using Relevant IC
2. Design Excess-3 to 9-Complement convertor using only four Full Adders and test the Circuit.
3. Design an Experimental model to demonstrate the operation of 74154 De-Multiplexer using LEDs for outputs.